

Curriculum Vitae

1. Personal Information

Name: Eduard Ayguadé Parra

Studies: Telecommunications Engineering from UPC, 1986. PhD in Computer Science from UPC, 1989.

Affiliation 1: Full Professor (since 1997)
Technical University of Catalunya(UPC)
Computer Architecture Department

Affiliation 2: Associate Director (since 2006)
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2. R&D Projects

2.1 National projects

- Diseño de Arquitecturas Paralelas de Alta Velocidad a Bajo Coste (PA85-0314), Spanish Ministry of Education, 1985-1989. Researcher.
- Diseño e Implementación de un Sistema Multiprocesador con Buses Multiplexados, Spanish Telephone Company (Telefonica), 1985-1986. Researcher.
- Sistema Multiprocesador Fuertemente Acoplado, Institut Català de Tecnologia, 1989-1991. Researcher.
- Arquitectura, Herramientas de Programación y Sistemas Operativos para Multiprocesadores (TIC 89-392), Spanish Ministry of Education, 1990-1992. Researcher.
- Arquitectura y Compilación para Supercomputadores (TIC 92-880), Spanish Ministry of Education, 1992-1995. Researcher and coordinator of the “Compiler for Parallel Architectures” activities.
- Acción Integrada Hispano-Britanica 1995-1996: Distribución Automática de Datos para Computadores de Altas Prestaciones (HB163-B), Spanish Ministry of Education, 1995-1996. Project coordinator.
- Computación de Altas Prestaciones (TIC 95-429), Spanish Ministry of Education, 1995-1998. Researcher and coordinator of the “Compiler for Parallel Architectures” activities.
- Computación Paralela para el Modelado de Problemas Industriales (TIC96-1630-CE), Spanish Ministry of Education, 1996- 1999. Project coordinator.
- Acción Integrada Hispano-Austriaca 1997: Técnicas Avanzadas para la Distribución de Datos (HU1996-10), Spanish Ministry of Education, 1997. Project coordinator.
- Explotación de Paralelismo y Multiprogramación (TIC97-1445-CE), Spanish Ministry of Education, 1997-2000. Project coordinator.
- Acció Integrada ACI amb University of Illinois 1997: High Performance Compilers, Catalan Government, 1997. Project coordinator.
- Acció Integrada ACI amb University of California at Santa Cruz 1998: Multithreaded Architectures, Catalan Government, 1998. Project coordinator.
- Acció Integrada ACI amb University of Illinois 1998: High Performance Compilers for Multithreaded Architectures, Catalan Government, 1998. Project coordinator.
- Computación de Altas Prestaciones II (TIC 98-511), Spanish Ministry of Education 1998- 2001. Researcher and coordinator of the “Compiler for Parallel Architectures” activities. Researcher and coordinator of the “Compiler for Parallel Architectures” activities.
- Computación de Altas Prestaciones III (TIC2001-0995), Spanish Ministry of Education 2002-2004. Researcher and coordinator of the “Compiler for Parallel Architectures” activities.
- Computación de Altas Prestaciones IV (TIN2004-07739), Spanish Ministry of Science and Technology 2004-2007. Researcher and coordinator of the “Programming Models and Compilers” activities.

- Supercomputación y eCiencia Consolider Program (CSD2007-00050), Spanish Ministry of Science and Innovation. 2007- 2012.
- Computación de Altas Prestaciones V (TIN2007-60625), Spanish Ministry of Science and Technology 2007-2012. Consolider project. Researcher and coordinator of the “Programming Models and Compilers” activities.
- Grup de Recerca Consolidat MPEXP (Models de Programació i Entorns d’Execució Paral·lels) (2009 SGR980). Generalitat de Catalunya, Dep. d’Innovació, Universitats i Empresa. October 2009-September 2012.

2.2 EU projects

- Performance-Critical Applications of Parallel Architectures APPARC, Basic Research Action BRA 6634, European Commission ESPRIT III, 1992-1995. Researcher.
- Advanced Computer Training and Technology Transfer, ACT- UETP University Enterprises Training Partnership, European Commission COMETT 92/1/7414/Ca, 1992-1994. Researcher.
- Training in Advanced Computing Applications, Tools and Architectures, ACT-UETP University Enterprises Training Partnership, European Commission COMETT 94/1/8353/Ca, 1994-1995. Researcher.
- PARANDES - Parallel Software for Applications in Chilean Industry, European Commission ESPRIT ITDC’94, 1995-1997. Researcher.
- PARALIN - Parallel Computing Modelling for Industrial Problems, European Commission INCO-DC, 1996-1998. Researcher.
- NANOS - Effective Integration of Fine-grain Parallelism Exploitation and Multiprogramming, European Commission ESPRIT Long Term Research LTR 21907, 1996-1999. Researcher.
- INTONE – Innovative OpenMP Tools for Non-experts (IST-1999-20252), European Comisión (Information Society Technologies). 2000-2003. Project coordinator.
- POP – Performance Portability of OpenMP (IST-2001-33071) , European Comisión (Information Society Technologies). 2001-2004. Researcher.
- SARC – Scalable Computer Architecture. EU Commission. Information Society Technologies, IST-2006-27648. January 2006 - December 2009. Researcher.
- ACOTES – Advanced Compiler Technologies for Embedded Streaming. EU Commission, Information Society Technologies, IST-2006-034869. June 2006 - May 2009. Researcher.
- VELOX – An Integrated Approach to Transactional Memory on Multi- and Many-core Computers. EU Commission, Information Society Technologies, IST-2007-216852. January 2008-December 2010.
- HiPEAC-2 Network of Excellence (High-performance and Embedded Architectures and Compilers). European Union Computing Systems, FP7/ICT 217068. February 2008-January 2012.
- HPC-Europa2, Pan-European Research Infrastructure on High-Performance Computing, JRA2 HPC on Massively Parallel Architectures: Programming models. European Union Research Infrastructures Initiative, contract no. 228398. January 2009-December 2010.
- TERAFLUX -- Exploiting Dataflow Parallelism in Teradevice Computing. EU Commission, Information Society Technologies, IST-2007-249013. January 2010-December 2013.
- EnCORE -- ENabling technologies for a programmable many-CORE. EU Commission, Information Society Technologies, IST-2007-248647. March 2010-February 2013. Researcher.
- TEXT – Towards Exaflop applicaTions. EU Commission, Information Society Technologies, IST-2007-261580. June 2010-May 2013. Researcher.

2.3 Contracts/projects with companies

- Automatic Data Distribution for the CONVEX SPP, CONVEX Computer Corporation and CONVEX Supercomputer S.A.E, 1992-1995. Project Leader.
- Integrating Data and Work Distribution in the Exemplar Systems, CONVEX Computer Corporation and CONVEX Supercomputer S.A.E, 1995. Project Leader.
- IBM Faculty Partnership Award. IBM International Business Machines Corporation. 5/2001-4/2002. Award recipient.
- MPI Scalability and Virtual Node for BG/L. IBM T.J. Watson. 3/2003-2/2005. Project coordinator.
- IBM Faculty Partnership Award. IBM International Business Machines Corporation. 6/2003-5/2004. Award recipient.
- IBM Faculty Partnership Award. IBM International Business Machines Corporation. 6/2004-5/2005. Award recipient.
- BSC-IBM SOW: Cell Programming Models. IBM Research Watson. June 2006 - May 2008. SOW coordinator.

- BSC-IBM SOW: Adaptive Systems. IBM Research Watson. December 2006 - November 2008. Researcher
- BSC-Microsoft: Transactional Memory and Multicore Systems. Microsoft Research. January 2007 - December 2008. Researcher
- BSC-IBM MareIncognito project. IBM Research. July 2007-October 2011. “Programming Models” workpackage leader.
- Programming models and tools for heterogeneous multicore systems. US Air Force, contract num. FA8655-09-1-3075. June 2009-May 2010. Researcher.
- BSC-Microsoft: Programming models for distributed multicore architectures. Microsoft Research. June 2010 - May 2012. Project leader.

3. Publications (Active research topics)

3.1 Compiler and runtime support for multicore programming models

- David Ródenas, Xavier Martorell, Eduard Ayguade, Jesús Labarta, George Almási, Calin Cascaval, José Castañós, Jose Moreira. Optimizing NANOS OpenMP for the IBM Cyclops Multithreaded Architecture. 19th International Parallel and Distributed Processing Symposium, April 2005.
- David Ródenas, Xavier Martorell, Eduard Ayguadé, Jesus Labarta, George Almási, Calin Cascaval, José Castañós, and José Moreira. Multilevel Parallelism using OpenMP on a Massive Multithreaded Architecture. Journal of Embedded Computing, Special issue: Issues in embedded single-chip multicore architectures, Vol 2(2), pp.141-155. April 2006.
- Tim Harris, Adrian Cristal, Osman S. Unsal, Eduard Ayguade, Simon P. Jones, Fabrizio Gagliardi, Burton Smith and Mateo Valero. Transactional Memory: An Overview. IEEE Micro. Hot Tutorials Special Issue. Vol. 27, Issue 3. pp. 8-29. May/June 2007.
- Miloš Milovanović, Roger Ferrer, Osman S. Unsal, Adrian Cristal, Xavier Martorell, Eduard Ayguadé, Jesús Labarta and Mateo Valero. Transactional Memory and OpenMP. International Workshop on OpenMP (IWOMP 2007). Beijing, China. June 2007. In Lecture Notes in Computer Science, vol. 4935, pp. 37-53. ISBN 0302-9743. Springer-Verlag, 2008.
- Paul Carpenter, David Rodenas, Xavier Martorell, Alex Ramirez, Eduard Ayguade. An streaming machine description and programming models. SAMOS VII: International Symposium on Systems, Architectures, Modeling and Simulation, Samos, Greece. Embedded Computer Systems: Architectures, Modeling, and Simulation, LNCS vol. 4599/2007, pp. 107-116. Springer. July 2007.
- Ferad Zyulkyarov, Osman S Unsal, Adrian Cristal, Milos Milovanovic, Eduard Ayguade and Mateo Valero. Memory Management for Transaction Processing Core in Heterogeneous Chip-Multiprocessors. OSHMA 2007: Workshop on Operating System support for Heterogeneous Multicore Architectures. In conjunction with Parallel Architectures and Compilation Techniques (PACT-2007). Brasov, Rumania. September 2007.
- Miloš Milovanović, Roger Ferrer, Vladimir Gajinov, Osman S. Unsal, Adrian Cristal, Eduard Ayguadé and Mateo Valero. Multithreaded Software Transactional Memory and OpenMP. MEDEA 2007: MEMory performance Workshop: DEaling with Applications, systems and architecture. In conjunction with Parallel Architectures and Compilation Techniques (PACT-2007). Brasov, Rumania. September 2007.
- Jairo Balart, Marc Gonzalez, Xavier Martorell, Eduard Ayguade, Zehra Sura, Tong Chen, Tao Zhang, Kevin O’Brien and Kathryn O’Brien. A Novel Asynchronous Software Cache Implementation for the Cell-BE Processor. LCPC 2007: 20th International Workshop on Languages and Compilers for Parallel Computing. Urbana (IL), USA. October 2007. In Lecture Notes in Computer Science, vol. 5234/2008, pp. 125-140. ISBN 0302-9743 . Springer-Verlag, 2008.
- Milos Milovanovic, Roger Ferrer, Vladimir Gajinov, Osman S. Unsal, Adrián Cristal, Eduard Ayguadé, Mateo Valero. Nebelung: Execution Environment for Transactional OpenMP. International Journal of Parallel Programming vol. 36 no. 3. pp. 326-346. ISSN: 0885-7458. Springer, 2008.
- Nikola Vujic, Marc Gonzalez, Xavier Martorell and Eduard Ayguadé. Automatic Pre-Fetch and Modulo Scheduling Transformations for the Cell BE Architecture. 21st Annual Workshop on Languages and Compilers for Parallel Computing (LCPC). University of Alberta. July 31- August 2, 2008. In Lecture Notes in Computer Sciences, vol. 5335/2008, Springer-Verlag, 2008.
- Ferad Zyulkyarov, Sanja Cvijic, Osman Unsal, Adrian Cristal, Eduard Ayguadé, Tim Harris and Mateo Valero. WormBench - A Configurable Workload for Evaluating Transactional Memory Systems. MEDEA -- MEMory performance: DEaling with Applications, systems and architecture (workshop held in conjunction with PACT-2008). Toronto, Canada. October 25-29, 2008.
- Marc Gonzalez, Nikola Vujic, Xavier Martorell, Eduard Ayguadé, Alexandre E. Eichenberger, Tong Chen, Zehra Sura, Tao Zhang, Kevin O’Brien, and Kathryn O’Brien. Hybrid Access-Specific

- Software Cache Techniques for the Cell BE Architecture. The 17th International Conference on Parallel Architectures and Compilation Techniques (PACT). Toronto, Canada. October 25-29, 2008.
- Roger Ferrer, Marc Gonzalez, Federico Silla, Xavier Martorell, Eduard Ayguadé. Evaluation of Memory Performance on the Cell BE with the SARC Programming Model. MEDEA -- MEMory performance: DEaling with Applications, systems and architecture (workshop held in conjunction with PACT-2008). Toronto, Canada. October 25-29, 2008.
 - Rosa M. Badia, Josep M. Perez, Eduard Ayguadé and Jesus Labarta. Impact of the memory hierarchy on shared memory architectures in multicore programming models. The 17th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing, 18-20 February 2009, Weimar (Germany).
 - Ferad Zyulkyarov, Vladimir Gajinov, Osman Unsal, Adrian Cristal, Eduard Ayguadé, Tim Harris, Mateo Valero. Atomic Quake: Using Transactional Memory in an Interactive Multiplayer Game Server. 14th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. February 14-18, 2009, Raleigh, North Carolina (USA).
 - Chinmay Kulkarni, Osman Unsal, Adrian Cristal, Eduard Ayguadé, Mateo Valero. Turbocharging boosted transactions or: How I Learnt to Stop Worrying and Love Longer Transactions. 14th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming. February 14-18, 2009, Raleigh, North Carolina (USA).
 - V. Gajinov, F. Zyulkyarov, A. Cristal, O. Unsal, E. Ayguadé, T. Harris, and M. Valero. QuakeTM: Parallelizing a Complex Serial Application Using Transactional Memory. 23rd International Conference on Supercomputing, June 8-12, 2009. Yorktown Heights, NY, USA
 - Vicenç Beltran, Xavier Martorell, Jordi Torres and Eduard Ayguadé. Accelerating Software Memory Compression on the Cell/B.E. Workshop on Hardware Accelerators for High Performance Computing (WAHA, collocated with ICS 2009). June 8, 2009. Yorktown Heights, NY, USA.
 - Paul Carpenter, Alex Ramirez and Eduard Ayguadé. The Abstract Streaming Machine: Compile-time performance modelling of stream programs on heterogeneous multiprocessors. SAMOS Workshop - International Workshop on Systems, Architectures, Modeling, and Simulation. Samos, Greece, July 20-23, 2009.
 - Judit Planas, Rosa M. Badia, Eduard Ayguadé and Jesus Labarta. Hierarchical task based programming with StarSs. International Journal of High Performance Computing Applications. Vol. 23, no. 3, pp. 284-299. July 2009.
 - Eduard Ayguadé, Rosa M. Badia, Francisco Igual-Peña, Jesús Labarta, Rafael Mayo, Enrique Quintana-Orti. An Extension of the StarSs Programming Model for Platforms with Multiple GPUs. Euro-Par 2009, Delft (The Netherlands), August 25-28, 2009.
 - Nikola Vujic, Lluc Alvarez, Marc Gonzalez, Xavier Martorell and Eduard Ayguadé. Adaptive and Speculative Memory Consistency Support for Multi-core Architectures with Local Memories. 22nd International Workshop on Languages and Compilers for Parallel Computing, University of Delaware, Newark, Delaware, USA. October 8-10, 2009.
 - Roger Ferrer, Alejandro Duran, Xavier Martorell and Eduard Ayguadé. Unrolling Loops Containing Task Parallelism. 22nd International Workshop on Languages and Compilers for Parallel Computing, University of Delaware, Newark, Delaware, USA. October 8-10, 2009.
 - Paul Carpenter, Alex Ramirez and Eduard Ayguadé. Mapping Stream Programs onto Heterogeneous Multiprocessor Systems. Proceedings of CASES 2009: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems, pp. 57-66. October 11-16, 2009. Grenoble (France).
 - Jesús Labarta, Eduard Ayguadé and Mateo Valero. BSC Vision Towards Exascale. International Journal of High Performance Computing Applications. Vol. 23, no. 4, pp. 340-343. October 2009.
 - Vicenç Beltran, David Carrera, Jordi Torres and Eduard Ayguadé. CellMT: A Cooperative Multithreading Library for the Cell/B.E. 16th Annual International Conference on High Performance Computing (HiPC-2009). December 16-19, 2009. Kochi, Cochin (India).
 - Nikola Vujic, Felipe Cabarcas, Marc Gonzalez, Alex Ramirez, Xavier Martorell and Eduard Ayguadé. DMA++: On the Fly Data Realignment for On-Chip Memories. The 16th IEEE International Symposium on High-Performance Computer Architecture (HPCA-16). Bangalore, India. January 9-14, 2010.
 - Roger Ferrer, Vicenç Beltran, Marc González, Xavier Martorell and Eduard Ayguadé. Analysis of Task Offloading for Accelerators. HiPEAC 2010 -- International conference on High-Performance Embedded Architectures and Compilers. Pisa, Italy. January 25-27, 2010.
 - Paul Carpenter, Alex Ramirez and Eduard Ayguadé. Buffer sizing for self-timed stream programs on heterogeneous distributed memory multiprocessors. HiPEAC 2010 -- International conference on High-Performance Embedded Architectures and Compilers. Pisa, Italy. January 25-27, 2010.

- Ramon Bertran, Marc Gonzalez, Xavier Martorell, Nacho Navarro and Eduard Ayguadé. Local Memory Design Space Exploration for High Performance Computing. *The Computer Journal*, Oxford University Press. DOI: 10.1093/comjnl/bxq026. March 2010.
- Nikola Vujic, Marc Gonzalez, Xavier Martorell and Eduard Ayguadé. Automatic Prefetch and Modulo Scheduling Transformations for the Cell BE Architecture. *IEEE Transactions on Parallel and Distributed Systems*, vol. 21, no. 4, pp. 494-505. April 2010.
- Ramon Bertran, Marc Gonzalez, Xavier Martorell, Nacho Navarro and Eduard Ayguadé. Decomposable and Responsive Power Models for Multicore Processors using Performance Counters. *ICS-2010 – 24th ACM International Conference on Supercomputing*, Tsukuba, Japan. June 1-4, 2010.
- Yoav Etsion, Alex Ramirez, Rosa M. Badia, Eduard Ayguade, Jesus Labarta, Mateo Valero. Task Superscalar: Using Processors as Functional Units. *HotPar'10 – 2nd USENIX Workshop on Hot Topics in Parallelism*, Berkeley (CA), USA. June 14-15, 2010.
- Harm Munk, Eduard Ayguadé, Cédric Bastoul, Paul Carpenter, Zbigniew Chamski, Albert Cohen, Marco Cornero, Philippe Dumont, Marc Duranton, Mohammed Fellahi, Roger Ferrer, Razya Ladelsky, Menno Lindwer, Xavier Martorell, Cupertino Miranda, Dorit Nuzman, Andrea Ornstein, Antoniu Pop, Sebastian Pop, Louis-Noël Pouchet, Alex Ramírez, David Ródenas, Erven Rohou, Ira Rosen, Uzi Shvadron, Konrad Trifunovic and Ayal Zaks. ACOTES Project: Advanced Compiler Technologies for Embedded Streaming. *International Journal on Parallel Programming*, published online June 2010. DOI 10.1007/s10766-010-0132-7
- Paul Carpenter, Alex Ramirez and Eduard Ayguadé. StarSsCheck: A Tool to Find Errors in Task-based Parallel Programs. *EuroPar-2010, Ischia (Italy)*. August 31st – September 3rd, 2010.
- Alessandro Cilardo, Luigi Esposito, Antonio Veniero, Antonino Mazzeo, Vicenç Beltran and Eduard Ayguadé. A CellBE-based HPC Application for the Analysis of Vulnerabilities in Cryptographic Hash Functions. *12th IEEE International Conference on High Performance and Communications (HPCC'10)*, Melbourne (Australia). September 1-3, 2010.
- Roger Ferrer, Pieter Bellens, Vicenc Beltran, Marc Gonzalez, Xavier Martorell, Rosa M. Badia, Eduard Ayguade, Jae-Seung Yeom, Scott Schneider, Konstantinos Koukos, Michail Alvanos, Dimitros S. Nikolopoulos, Angelos Bilas. *Parallel Programming Models for Heterogeneous Multicore Architectures*. *IEEE Micro*, vol. 30, no. 5, Special Issue “Multicore: The View from Europe”, pp. 42-53, Sep./Oct. 2010.
- Yoav Etsion, Felipe Cabarcas, Alejandro Rico, Alex Ramirez, Rosa M. Badia, Eduard Ayguadé, Jesus Labarta and Mateo Valero. Task Superscalar: An Out-of-Order Task Pipeline. *43rd International Symposium on Microarchitecture (MICRO-43)*. Atlanta, Georgia (USA), December 2010.
- Mauricio Araya-Polo, Javier Cabezas, Mauricio Hanzich, Miquel Pericas, Félix Rubio, Isaac Gelado, Muhammad Shafiq, Enric Morancho, Nacho Navarro, Eduard Ayguade, José María Cela and Mateo Valero. Assessing Accelerator-based HPC Reverse Time Migration. *IEEE Transactions on Parallel and Distributed Systems*, special issue High-Performance Computing with Accelerators, vol. 22, no. 1, pp. 147-162, January 2011.
- Nikola Vujic, Felipe Cabarcas, Marc Gonzalez, Alex Ramirez, Xavier Martorell and Eduard Ayguadé. DMA++: On the Fly Data Realignment for On-Chip Memories. *IEEE Transactions on Computers*. To be published, 2011.
- Alejandro Duran, Eduard Ayguadé, Rosa M. Badia, Jesús Labarta, Luis Martinell, Xavier Martorell and Judit Planas. OmpSs: a Proposal for Programming Heterogeneous Multi-core Architectures. *International Journal of High Performance Computing Applications (IJHPCA)*. To be published, 2011.

3.2 Compiler and runtime support for shared-memory programming models (OpenMP)

- X. Martorell, J. Labarta, J.I. Navarro and E. Ayguadé, A Library Implementation of the Nano-Threads Programming Model. *Euro-Par'96*, Lyon (France). *Lecture Notes in Computer Science*, Springer-Verlag. Vol. 1124, pp. 644-649. August 1996.
- X. Martorell, J. Labarta, J.I. Navarro and E. Ayguadé, Analysis of Several Scheduling Algorithms under the Nano-Threads Programming Model. *11th IEEE International Parallel Processing Symposium IPPS'97*, Geneve (Suiza). *Lecture Notes in Computer Science*, Springer-Verlag. Vol. 1124, pp. 644-649. April 1997.
- E. Ayguadé, X. Martorell, J. Labarta, M. Gonzalez and J.I. Navarro, Exploiting Parallelism Through Directives on the Nano-Threads Programming Model. *10th Workshop on Programming Languages and Compilers for Parallel Computing*, Minneapolis (USA), August 1997.

- X. Martorell, E. Ayguadé, N. Navarro, J. Corbalan, M. Gonzalez and J. Labarta, Thread Fork/join Techniques for Multi-level Parallelism Exploitation in NUMA Multiprocessors. 13th International Conference on Supercomputing (ICS'99), Rhodes (Greece). June 1999.
- X. Martorell, E. Ayguadé, J. Labarta and N. Navarro, Improving the Performance of Multiprogrammed Workloads in Origin2000 Systems. 5th European Cray/SGI MPP Workshop, Bologna (Italy). September 1999.
- E. Ayguadé, X. Martorell, J. Labarta, M. Gonzalez and N. Navarro, Exploiting Multiple Levels of Parallelism in OpenMP: A Case Study. 29th Annual International Conference on Parallel Processing (ICPP'99), Aizu (Japan). September 1999.
- E. Ayguadé, M. Gonzalez, J. Labarta, X. Martorell, N. Navarro, J. Oliver, NanosCompiler: A Research Infrastructure for OpenMP Extensions. 1st European Workshop on OpenMP (EWOMP'99), Lund (Sweden). September/October 1999.
- M. Gonzalez, X. Martorell, J. Oliver, E. Ayguadé and J. Labarta, Code Generation and Run-time Support for Multi-level Parallelism Exploitation. 8th International Workshop on Compilers for Parallel Computing (CPC'00), Aussois (France). January 2000.
- M. Gonzalez, X. Martorell, J. Oliver, A. Serra, E. Ayguadé, J. Labarta and N. Navarro, Applying Interposition Techniques for Performance Analysis of OpenMP Parallel Applications. IEEE 2000 International Parallel and Distributed Processing Symposium (IPDPS'2000), Cancun (Mexico). May 2000.
- J. Oliver, E. Ayguadé and N. Navarro, Towards an Efficient Exploitation of Loop-level Parallelism in Java. ACM Java Grande 2000 Conference, San Francisco CA (USA). June 2-4, 2000.
- J. Oliver, E. Ayguadé, N. Navarro, J. Guitart, J. Torres and J. Labarta. Strategies for the Efficient Exploitation of Loop-level Parallelism in Java. Concurrency and Computation: Practice and Experience (Java Grande 2000 Special Issue). Vol. 13(8-9). pp. 663-680. July 2001.
- M. Gonzalez, J. Oliver, X. Martorell, E. Ayguadé, J. Labarta and N. Navarro, OpenMP Extensions for Thread Groups and Their Run-time Support. 13th International Workshop on Languages and Compilers for Parallel Computing (LCPC'2000), New York (USA). August, 2000. Also in Languages and Compilers for Parallel Computing. Lecture Notes in Computer Science LNCS 2017. S.P. Midkiff, J.E. Moreira, M. Gupta, S. Chatterjee, J. Ferrante, J. Prins, W. Pugh, C.-W. Tseng (Eds.). pp. 324-338. 2001.
- M. Gonzalez, J. Oliver, X. Martorell, E. Ayguadé, J. Labarta and N. Navarro, Precedence Relations in the OpenMP Programming Model. 2nd European Workshop on OpenMP (EWOMP'00), Edimburgh (UK), September 2000.
- J. Labarta, E. Ayguadé, J. Oliver and D. Henty, New OpenMP Directives for Irregular Data Access Loops. 2nd European Workshop on OpenMP (EWOMP'00), Edimburgh (UK), September 2000.
- M. Gonzalez, E. Ayguadé, X. Martorell, J. Labarta, N. Navarro and J. Oliver, NanosCompiler: Supporting Flexible Multilevel Parallelism in OpenMP. Concurrency: Practice and Experience. Special issue on OpenMP. vol. 12, no. 11. November 2000.
- M. Gonzalez, E. Ayguadé, X. Martorell and J. Labarta. Defining and Supporting Pipelined Executions in OpenMP. 2nd International Workshop on OpenMP Applications and Tools. July 2001. OpenMP Shared Memory Parallel Programming, R. Eigenmann and M. Voss (Eds.), Lecture Notes on Computer Science LNCS 2104, pp. 155-169, Springer. 2001.
- D. Nikolopoulos, E. Artiaga, E. Ayguadé and J. Labarta. Exploiting Memory Affinity in OpenMP through Schedule Reuse. 3rd European Workshop on OpenMP (EWOMP'01) in conjunction with the 10th International Conference on Parallel Architectures and Compilation Techniques (PACT'01). Barcelona (Spain) September 2001. Also in ACM SIGARCH Computer Architecture News. Vol. 29, no. 5, pp. 49-55, ACM Press, December 2001.
- E. Ayguadé, M. Brorsson, H. Brunst, H.-C. Hoppe, S. Karlsson, X. Martorell, W.E. Nagel, F. Schlimbach, G. Utrera and M. Winkler. OpenMP Performance Analysis Approach in the INTONE Project. 3rd European Workshop on OpenMP (EWOMP'01) in conjunction with the 10th International Conference on Parallel Architectures and Compilation Techniques (PACT'01). Barcelona (Spain) September 2001.
- H. Jin, G. Jost, J. Yan, E. Ayguadé, M. Gonzalez and X. Martorell. Automatic Multilevel Parallelization Using OpenMP. 3rd European Workshop on OpenMP (EWOMP'01) in conjunction with the 10th International Conference on Parallel Architectures and Compilation Techniques (PACT'01). Barcelona (Spain) September 2001. Also in Scientific Programming. Vol. 11, no. 2. pp. 177-190. June 2003.
- M. Gonzalez, E. Ayguadé, X. Martorell and J. Labarta. Complex Pipelined Executions in OpenMP Parallel Applications. International Conference on Parallel Processing (ICPP'01). September 2001.

- D. Nikolopoulos, E. Ayguadé and C. D. Polychronopoulos. Scaling Irregular Parallel Codes with Minimal Programming Effort. REF. REVISTA/LIBRO: ACM/IEEE Supercomputing'2001: High Performance Networking and Computing Conference (SC'2001). Denver, Colorado (USA). November 2001.
- J. Labarta, E. Ayguade, J. Oliver and D. Henty. New OpenMP Directives for Irregular Data Access Loops. Scientific Programming. Vol. 9, no. 2-3. IOS Press, March 2002.
- M. González, E. Ayguadé, X. Martorell, J. Labarta and P-V. Luong. Dual-Level Parallelism Exploitation with OpenMP in Coastal Ocean Circulation Modeling. 2nd Workshop on OpenMP: Experiences and Implementations (WOMPEI'02 part of ISHPC-02). Kyoto (Japan), May 2002. Published in Lecture Notes in Computer Science LNCS 2327, Springer. May 2002.
- D. S. Nikolopoulos, E. Ayguadé and C. D. Polychronopoulos. Runtime vs. Manual Data Distribution for Architecture-agnostic Shared-memory Programming Models. International Journal of Parallel Programming, vol. 30, no. 4. Plenum Publishing Corporation. August 2002.
- E. Artiaga, N. Navarro, E. Ayguade, J. Labarta. Dynamic Loop Schedulers and Memory Behavior. Fourth European Workshop on OpenMP (EWOMP 2002). Rome, Italy, September 2002.
- D. S. Nikolopoulos, E. Artiaga, E. Ayguadé and J. Labarta. Scaling Non-Regular Shared-Memory Codes by Reusing Custom Loop Schedules. Scientific Programming. Scientific Programming. Vol. 11, no. 2. pp. 143-159. June 2003.
- Eduard Ayguade, Bob Blainey, Alejandro Duran, Jesus Labarta, Francisco Martinez, Xavier Martorell and Raul Silvera. Is the SCHEDULE Clause Really Necessary in OpenMP? International Workshop on OpenMP Applications and Tools. June 2003. M.J. Voss (Editor), Lecture Notes on Computer Science, vol. LNCS 2716, pp. 69–83. Springer-Verlag. 2003.
- George Almasi, Eduard Ayguade, Calin Cascaval, Jose Castanos, Jesus Labarta, Francisco Martinez, Xavier Martorell and Jose Moreira. Evaluation of OpenMP for the Cyclops Multithreaded Architecture. International Workshop on OpenMP Applications and Tools. June 2003. M.J. Voss (Editor), Lecture Notes on Computer Science, vol. LNCS 2716, pp. 147–159. Springer-Verlag. 2003.
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4.4 Loop transformations and parallelization

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5. Organization of Conferences and Special Issues in Journals

- 1^{as} Jornadas de Paralelismo, Organizing committee. Sitges (Barcelona), 1990.
- 2nd International Workshop on Massive Parallelism: Hardware, Software and Applications, Organizing and programme committee. Capri (Italy), 1994.
- 9th ACM International Conference on Supercomputing ICS'95, Local Arrangements and Registration Chair. Barcelona (Spain), 1995. Grants from Spanish Ministry of Education "Programa Sectorial de Promoción del Conocimiento-1995", and Catalan Government "Accions Mobilitzadores" (CIRIT-1994 and CIRIT-1995).
- XV International Conference of the Chilean Computer Science Society SCCC'95, Program committee. Arica, Chile. 1995.
- Eighth IEEE Symposium on Parallel and Distributed Processing SPDP'96, Program committee. New Orleans (Louisiana-USA). 1996.
- II Jornadas de Informática, Asociación Española de Informática y Automática. Program committee. Granada (Spain), 1996.
- Workshop on Automatic Data Layout and Performance Prediction AP'97, Steering Committee chair and organizing committee. Barcelona (Spain), 1997.
- International Symposium on Computer Architecture ISCA'98, Local arrangements and registration chair. Barcelona (Spain), 1998. Grants from Spanish Ministry of Education "Acciones Especiales TIC-1998", and Catalan Government "Accions Mobilitzadores" (CIRIT-1997).
- 13th ACM International Conference on Supercomputing ICS'99, Publicity chair and program committee. Rhodes (Greece), 06/99.
- 29th Annual International Conference on Parallel Processing ICPP'99, Session chair. Aizu, Japan, 09/99.
- 14th ACM International Conference on Supercomputing ICS'00, Publicity chair. New Mexico (USA), 06/00.
- 30th Annual International Conference on Parallel Processing ICPP'2000. Program Committee member. Toronto (Canada), 09/2000.

- 3rd International Symposium on High-Performance Computing ISHPC2K. Organizing Committee and Chair for the “International Workshop on OpenMP: Experiences and Implementations”, 10/2000.
- 7th International Conference on High Performance Computing HiPC’00. Publicity chair and Program Committee member. Bangalore (India), 12/2000.
- 2nd European Workshop on OpenMP (EWOMP’2000). Program Committee, Keynote session chair and Panel Session participant. Univ. of Edimburgh, Scotland - UK (9/2000).
- Compilers and Operating Systems for Low Power (PACT’00). Program Committee. Philadelphia, USA (10/2000).
- 15th International Conference on Supercomputing ICS’2001. Organizing Committee (Publicity Chair). Sorrento, Italy (5/2001).
- EUROPAR’01 (Instruction-level Parallelism and Architecture Track). Program Vice-chair. Manchester, UK, (8/2001)
- 31st Annual International Conference on Parallel Processing ICPP’2001. Organizing Committee (Program Committee Web Master Chair). Valencia, Spain (9/2001).
- Parallel Architectures and Compilation Techniques (PACT’01). Organizing Committee (Local Arrangements Co-chair and Conference Web Master). Barcelona, Spain, (9/2001). Grants from Spanish Ministry of Education (Acciones Especiales de la CICYT) and Catalan Government (CIRIT Ajuts per la Organització de Congressos).
- 3rd European Workshop on OpenMP (EWOMP’2001). General Chair. Barcelona, Spain, (9/2001).
- Workshop on Compilers and Operating Systems for Low Power (COLP’01). Program Committee. Barcelona, Spain, (9/2001)
- 2nd Workshop on OpenMP: Experiences and Implementations (WOMPEI’02 part of ISHPC-02). Program Chair. Kyoto, Japan (5/2002).
- 16th International Conference on Supercomputing (ICS’02). Publicity Co-chair and Program Committee. NY, USA (6/2002).
- 31st Annual International Conference on Parallel Processing (ICPP’02). Organizing Committee (Publicity Co-chair) and Program Committee. Vancouver, Canada, (8/2002).
- EUROPAR’02 (Compilers for High-Performance / Compilation and Parallelization Techniques Track). Program Vice-chair. Paderborn, Germany (8/2002)
- 11th Parallel Architectures and Compilation Techniques (PACT’02). Program Committee. Virginia, USA (9/2002).
- 2nd Workshop on Caching, Coherence and Consistency (WC3’02), part of PACT’02. Program Committee. Virginia, USA (9/2002).
- Fourth European Workshop on OpenMP (EWOMP 2002). Program Committee and Panel Session Organizer. Rome (Italy). September 2002.
- 2003 International Parallel and Distributed Processing Symposium (IPDPS). Program Committee. Nice (France). April 2003.
- 8th International Workshop on High-Level Parallel Programming Models and Supportive Environments, in conjunction with International Parallel and Distributed Processing Symposium (IPDPS-2003). Program Committee. Nice (France). April 2003.
- WOMPAT 2003: Workshop on OpenMP Applications and Tools. Program Committee. Toronto, Ontario Canada. June, 2003.
- First International Workshop on Heterogeneous and Adaptive Computing - "Challenges of Large Applications in Distributed Environments" (CLADE 2003), in conjunction with 12th IEEE International Symposium on High Performance Distributed Computing (HPDC-12). Program Committee. Seattle, Washington (USA). June 2003.
- E. Ayguadé. Special Issue on OpenMP. International Journal of Parallel Programming. Vol. 31, No. 3. June 2003. (Also includes Guest Editor’s Introduction, pp. 181-183).
- E. Ayguadé and B. Chapman. Special Issue on OpenMP. Scientific Programming. Vol. 11, no. 2. June 2003. (Also includes Guest Editor’s Foreword pp. 79-80).
- Fifth European Workshop on OpenMP (EWOMP 2003). Program Committee. Aachen (Germany). September 2003.
- 32nd Annual International Conference on Parallel Processing (ICPP’03). “Compilers and Languages” Vice-chair. Kaohsiung, Taiwan. October 2003.
- 9th International Workshop on High-Level Parallel Programming Models and Supportive Environments (HIPS’2004), in conjunction with International Parallel and Distributed Processing Symposium (IPDPS-2004). Program Committee. Santa Fe, USA. April 2004.
- Second International Workshop on Heterogeneous and Adaptive Computing - "Challenges of Large Applications in Distributed Environments" (CLADE 2004), in conjunction with 13th IEEE

- International Symposium on High Performance Distributed Computing (HPDC-12). Program Committee. Honolulu, Hawai. June 2004.
- Workshop on OpenMP Applications and Tools (WOMPAT 2004). Program Committee. Houston, USA. June 2004.
 - 33rd Annual International Conference on Parallel Processing (ICPP'04). Publicity chair. Montreal, Canada. August 2004.
 - 13rd Parallel Architectures and Compilation Techniques (PACT'04). Program Committee. Antibes Juan-les-Pins, France (29/9-3/10/2004)
 - 15th International Conference on Application-specific Systems, Architectures and Processors (ASAP'04). Program Committee. Galveston TX, USA (27-29/9/2004)
 - EWOMP 2004: European Workshop on OpenMP. Program Committee. Stockholm, Sweden (18-22/10/2004).
 - 3rd Workshop on OpenMP: Experiences and Implementations (WOMPEI'05). Program Committee. Tsukuba, Japan (20-21/1/2005).
 - 34th Annual International Conference on Parallel Processing (ICPP'05). Program Vice-Chair, "Compilers and Languages" track. Oslo, Norway (14-17/6/2005).
 - 10th IEEE Symposium on Computers and Communications (ISCC'05). Program Committee. Cartagena, Spain (27-30/6/2005).
 - 14th Parallel Architectures and Compilation Techniques (PACT'05). Publicity co-Chair. Saint Louis, Missouri (17-21/9/2005).
 - 3rd Int. Symposium on Parallel and Distributed Processing and Applications (ISPA'05). Program Committee. Nanjing, China, (2-5/11/2005).
 - 38th International Symposium on Microarchitecture (MICRO-38). Local Arrangements Chair. Barcelona, Spain (12-16/11/2005).
 - 2005 International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2005). Barcelona, Spain (17-18/11/2005). Local Arrangements Chair and Program Committee
 - 14th Euromicro Conference on Parallel, Distributed and Network-based Processing (PDP2006). Montbeliard-Sochaux, France (15-17/2/2006). Program Committee.
 - 20th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2006). Rhodes, Greece (25-29/4/2006). Program Committee
 - 2nd International Workshop on OpenMP (IWOMP-2006). Reims, France (12-15/6/2006). Program Committee.
 - The 20th ACM International Conference on Supercomputing (ICS 2006). Queensland, Australia (28/6 – 1/7/2006). Program Committee.
 - Issue 7: Parallel Computer Architecture and ILP. Euro-Par 2006 European Conference on Parallel Computing. Dresden, Germany (29/8 – 1/9/2006). Issue Global Chair.
 - The 2006 International Conference on High Performance Computing and Communications (HPCC 2006). Munich, Germany (13-15/9/2006). Program Committee
 - Workshop on Programming Models for Ubiquitous Parallelism (in conjunction with PACT'06). Seattle, Washington (16/9/2006). Program Committee
 - CASCON 2006: Dublin Symposium, In association with the 16th Annual International Conference on Computer Science and Software Engineering. Dublin, Ireland (16-17/10/2006). Program Committee.
 - 19th International Workshop on Languages and Compilers for Parallel Computing (LCPC 2006). New Orleans, Louisiana (USA) (2-4/11/2006). Program Committee.
 - 13th IEEE International Conference on High Performance Computing (HiPC 2006). Bangalore, India (18-21/12/2006). Program Committee.
 - 15th Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP 2007). Naples, Italy (7-9/2/2007). Program Committee
 - ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming (PPoPP'07). San Jose (CA), USA (14-17/3/2007). Program Committee.
 - E. Ayguadé, G. Baumgartner, J. Ramanujam, and P. Sadayappan (Eds.). Languages and Compilers for Parallel Computing. 18th International Workshop on Languages and Compilers for Parallel Computing (LCPC 2005), Hawthorne, NY, USA. Lecture Notes in Computer Science. Volume LNCS 4339/2006. Springer, ISBN: 978-3-540-69329-1. May 2007.
 - 3rd International Workshop on OpenMP (IWOMP-2007). Beijing, China (3-7/6/2007). Publications Co-Chair and Program Committee
 - 21st ACM International Conference on Supercomputing (ICS'07). Seattle area, USA (7/2007). Program Co-chair

- Eduard Ayguade and Matthias Mueller. Special Issue on OpenMP (vol. 1). International Journal of Parallel Programming, Vol. 35, No. 4, pp. 331-333. August 2007.
- 20th International Workshop on Languages and Compilers for Parallel Computing (LCPC 2007). University of Illinois at Urbana-Champaign, Chicago (USA) (11-13/10/2007). Program Committee
- MULTIPROG-2008 – First Workshop on Programmability Issues for Multi-Core Computers. Held in conjunction with the 3rd International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2008). Goteborg, Sweden (1/2008). Organizing committee.
- CC 2008 – International Conference on Compiler Construction. Budapest. Hungary (4/2008). Program Committee.
- IWOMP 2008 – 4th International Workshop on OpenMP. Purdue University, West Lafayette, IN (USA) (12-14/5/2008). Publications Co-Chair and Program Committee.
- ICS'08 – 22nd ACM International Conference on Supercomputing. Island of Kos, Greece (7-12/6/2008). Workshops and Tutorials Chair.
- LCPC 2008 – 21st International Workshop on Languages and Compilers for Parallel Computing. Edmonton, Alberta (Canada) (31/7-2/8/2008). Program Committee.
- ICPP 2008 – International Conference on Parallel Processing. Portland (OR), USA (8-12/9/2008). Program Committee (Compilers and Languages Track)
- MULTIPROG-2009 – Second Workshop on Programmability Issues for Multi-Core Computers. Held in conjunction with the 4th International Conference on High-Performance Embedded Architectures and Compilers (HiPEAC 2009). Paphos, Cyprus, (25-28/1/2009). Organizing committee.
- HiPEAC 2009 – The 4th International Conference on High Performance and Embedded Architectures. Paphos, Cyprus, (25-28/1/2009). Program Committee.
- IWOMP-2009 – 5th International Workshop on OpenMP. Technische Universität Dresden (Germany) (3-5/6/2009). Program Committee.
- LCPC 2009 – 22nd International Workshop on Languages and Compilers for Parallel Computing. University of Delaware, Newark, Delaware (USA) (8-10/10/2009). Program Committee.

6. Conferences and Seminars

- Experiences with Automatic Data Distribution, Convex User Group Worldwide Conference 1994. Dallas-Texas (USA), 1994.
- Automatic Data Distribution for the CONVEX Exemplar, European Convex User Conference 1994. Krakow, Poland, 1994.
- High Performance Fortran Languages and Basic Compilation Strategies. Tutorial in SUP'EUR95 High Performance Computing in Europe. Madrid (Spain) 1995.
- Arquitecturas y Compiladores para Computadores Paralelos. Tutorial in XV International Conference of the Chilean Computer Science Society. Arica - Chile, 1995.
- Ictineo: A Tool for Research on ILP. Research Exhibit “The Polaris Compiler: Use in Research and Education”. IEEE/ACM Supercomputing'96, Pittsburgh (PA), 1996.
- Arquitecturas Paralelas y Modelos de Programación. Tutorial in XVII International Conference of the Chilean Computer Science Society. Valparaiso - Chile, 1997.
- NanosCompiler: A Research Infrastructure for Multilevel Parallelism Exploitation in OpenMP. Invited talk at Waseda University. Tokyo – Japan, 1999.
- Research Exhibit “CEPBA - European Center for Parallelism of Barcelona”. IEEE/ACM Supercomputing'99, Portland (Oregon, USA), November 1999.
- Research Exhibit “CEPBA - European Center for Parallelism of Barcelona”. IEEE/ACM Supercomputing'00, Dallas (Texas, USA), November 2000.
- Programming Models for New Architectures. Seminar at the Universidad de la Laguna, Canary Islands (Spain), November 2000.
- Research Exhibit “CEPBA - European Center for Parallelism of Barcelona”. IEEE/ACM Supercomputing'01, Denver (CO, USA), November 2001.
- Self-analysis in Parallel Program Scheduling. IBM conference on Shaping the Information Society in Europe – 2002. April 2002.
- OpenMP Implementation and Performance Issues, Eduard Ayguade (CEPBA), Mats Brorsson (KTH), Sven Karlsson (KTH), Xavier Martorell (CEPBA) and Marc Gonzalez (CEPBA). Tutorial at the Fourth European Workshop on OpenMP (EWOMP 2002). Rome (Italy). September 2002.
- Performance Analysis Tools and Techniques. Panel session organizer and chair. Fourth European Workshop on OpenMP (EWOMP 2002). Rome (Italy). September 2002.
- Research Exhibit “CEPBA - European Center for Parallelism of Barcelona”. IEEE/ACM Supercomputing'02, Baltimore (USA). November 2002.

- What are the necessary ingredients of scalable OpenMP programming?. Panel session member. European Workshop on OpenMP (EWOMP'2003). Aachen (Germany). September 2003.
- Experiences in Exploiting Nested Parallelism in OpenMP. Invited talk. Workshop on OpenMP: Experiences and Implementations (WOMPEI'2003). Tokyo (Japan). October 2003.
- Programación de Arquitecturas Paralelas. Invited talk. Summer School at the Universidad de Castilla-La Mancha. July 7-9, 2004. Albacete (Spain)
- Arquitecturas y Modelos de Programación para Multicore. Invited talk with Alex Ramirez. Jornadas de Paralelismo. September 17, 2008. Castellon de la Plana (Spain).

7. PhD Students

- Jordi Torres i Viñals. Extracció Automàtica de Paral·lelisme en Bucles Seqüencials Numèrics amb Recurrencies. Advisor. Universitat Politècnica de Catalunya. 1993. (UPC Best Thesis Award, 1993).
- Montse Peiron Guàrdia. Optimització del Rendiment del Sistema de Memòria en Multiprocessadors Vectorials. Co-advisor with Prof. Mateo Valero. Universitat Politècnica de Catalunya. 1995.
- Josep Llosa Espuny. Reducing the Impact of Register Pressure on Software Pipelining. Co-advisor with Prof. Mateo Valero. Universitat Politècnica de Catalunya. 1996. (UPC Best Thesis Award).
- Jordi Garcia Alminyana. Distribución Automática de Datos en MPP. Advisor. Universitat Politècnica de Catalunya. 1997.
- Javier Zalamea León. Organization and Compiler Management of Register Files. Co-advisor with Josep Llosa. Universitat Politècnica de Catalunya. 2002.
- Daniel Ortega Fernandez. Memory Instruction Bypassing. Co-advisor with Mateo Valero. Universitat Politècnica de Catalunya. 2003.
- Marc Gonzalez Tallada. Multilevel Parallelism Exploitation in Shared-memory Multiprocessor Systems. Co-advisor with Xavier Martorell. Universitat Politècnica de Catalunya. 2003.
- Jordi Guitart. Performance Improvement of Multithreaded Java Applications Execution on Multiprocessor Systems. Co-advisor with Jordi Torres. Universitat Politècnica de Catalunya. 2005
- David Carrera Perez. Adaptive Execution Environments for Application Servers. Co-advisor with Jordi Torres. Universitat Politècnica de Catalunya. 2008
- Vicenç Beltran Querol. Improving Web Server Efficiency on Commodity Hardware. Co-advisor with Jordi Torres. Universitat Politècnica de Catalunya. 2008
- Alejandro Duran Gonzalez. Self-tuned Parallel Runtimes: a Case of Study for OpenMP. Co-advisor with Julita Corbalan. Universitat Politècnica de Catalunya. 2008
- PhD (Co)Advisor of Paul Carpenter (with Alex Ramirez), Vladimir Gajinov (with Osman Unsal), Nikola Vujic (with Marc Gonzalez), Muhammad Shafiq (with Miquel Pericas), Judit Planas, Rahul Gayatri and Vinoth Elangovan (with Rosa M. Badia).

8. Grants and awards

- Grant from Telefónica (España) to carry out the final engineering project "Diseño e Implementación de un Sistema Multiprocesador con Buses Multiplexados", 1985-86.
- Extraordinary PhD award "Doctor en Informática 1989", Universitat Politècnica de Catalunya, 1992.
- IBM Faculty Partnership Award for 2001 (award: \$40.000), 2003 (award: \$40.000) and 2004 (award: \$40.000).

9. Other issues

- Training manager at C⁴ (Centre de Computació i Comunicacions de Catalunya), 1996-1998.
- Responsible for PhD program at the Computer Architecture Department (UPC): 1997-1999 and since 2002.
- Board of Managers, Project Manager and Researcher of the CEPBA-IBM Research Institute (Barcelona), November 2000 – December 2004.
- Member of the cOMPunity, Inc. Board of Directors (The Community of OpenMP Users, Researchers, Tool Developers and Providers). Representative of cOMPunity in the Futures committee of the OpenMP ARB (Architecture Review Board), since October 2001.
- SUSP member (Scientific Users' Selection Panel). Transnational Access program. HPC-Europa (Pan-European Research Infrastructure on High Performance Computing), since 2004.